REMARKS

Claims 1-10, 25, 29, 33 and 35 are pending in this application. Claim 34 is withdrawn. By this Amendment, claims 1-10, 25 and 33-34 are amended, claim 35 is added, and claims 11-24, 26-28, and 30-32 are cancelled without prejudice or disclaimer. Reconsideration of the present application based on the above amendments and the following remarks is respectfully requested.

The Office Action rejects claims 1-10, 25, 29, and 33 under 35 U.S.C. §102(b) as being anticipated by European Patent Application No. EP 0 804 008 A2 to Baker. This rejection is respectfully traversed.

Claim 1

Baker fails to disclose a management circuit which manages an interface with a random accessible storage memory so that control information of a packet is written by a first upper layer into a control information area of the random accessible storage memory and data of the packet corresponding to the control information is written by a second upper layer into a data area different from the control information area of the random accessible storage memory, as claimed in claim 1. Support for this amendment may be found in the specification beginning on page 23, line 20.

There is no disclosure in Baker of managing an interface with random accessible storage memory (RAM) so that control information and data are written into separate memory areas.

Baker appears to be similar to a comparative example as illustrated in Fig. 8 of the present application. Comparing Fig. 8 of the present application and Fig. 2 of Baker, it is clear that 1) FIFOs 904, 906 and 908 in Fig. 8 correspond to respective FIFOs 80, 82 and 84 in Fig. 2 of Baker; 2) link core 902 in Fig. 8 of the present application corresponds to the link layer control logic 90 in Fig. 2 of Baker; and 3) the CPU interface 910 in Fig. 8 of the present

application corresponds to the PCI bus logic 60 in Fig. 2 of Baker. According to Baker, control information (header) of a packet and data, not separated from each other, is first written in FIFOs 80, 82 and 84 of Fig. 2 (FIFOs 904, 906 and 908 of Fig. 8 of the present application) and then read. More specifically, when packet 1 (header 1, data 1), packet 2 (header 2, data 2) and packet 3 (header 3, data 3) are to be transmitted, the transfer packets must be written in a transfer FIFO in the order of header 1, data 1, header 2, data 2, header 3 and data 3 as a FIFO stands for a first-in-first-out memory and not random accessible memory.

Fig. 15A of the present application, which is similar to the Baker approach, shows that the upper layer (firmware, CPU) creates control information (header) and writes it in a FIFO. Subsequently, data (for example, print data, image data) fetched from a device (for example, printer, digital camera) in the application layer (upper layer) is written in the FIFO. Finally, the upper layer (firmware) instructs the start of packet transmission at a timing indicated by an arrow in Fig. 15A.

In exemplary embodiments of the invention according to claim 1, on the other hand, a randomly accessible storage memory (for example, RAM 80 in Figs. 6 and 13) is separated into a control information area (header area) and a data area as shown in Figs. 7, 12 and 14. Therefore, as shown in Fig. 15B, the upper layer (firmware) may create the control information (header) and perform the writing processing of the control information area (header), while data is fetched from the application-layer device to the data area of the memory. Thus, the packet transmission start instruction may be issued at the timing shown by an arrow in Fig. 15B and data may be transferred much faster than the transmission as shown in Fig. 15A.

Because Baker does not disclose managing an interface so that control information and data are written into separate areas, data is transferred much slower when compared to a device according to claim 1. Thus, in order to speed up the data transfer, in Baker, packet control lists are built by the upper layer (firmware, CPU) (Fig. 20; pg. 17, lines 9 to 13). Baker does not

disclose managing an interface with random accessible storage memory so that control information and data are written into separate memory areas.

For at least the foregoing reasons, claim 1 is patentably distinct from Baker. Likewise, those claims which depend from claim 1 are distinguishable from Baker for at least the reasons discussed above, as well as for the additional reasons discussed below.

Claims 2-3 and 5-6

Baker fails to disclose a data transfer control device comprising a packet assembly circuit wherein the packet assembly circuit obtains a data pointer indicating an address of data that is to be read from a data area, from control information of a control information area of the random accessible storage memory, that has been read from the control information area, and uses the obtained data pointer to read data from the data area, as claimed in claim 2.

According to embodiments of claims 2-3 and 5-6, the upper layer (firmware) achieves automatic package assembly processing, as well as speeds up the processing, by writing a data pointer to the control information in the control information area of the RAM when creating control information. Baker fails to disclose these features.

Claim 3

Baker does not disclose a packet assembly circuit which reads control information of the packet from the control information area and utilizes a period of time during which the link circuit is creating error-checking information for the control information of the packet, to obtain a data pointer from control information.

For example, in exemplary embodiments of claim 3, as shown in Fig. 28, a data pointer is obtained from control information as shown by B11, utilizing a period during which the error-checking information (header CRC) is created. Baker fails to disclose these features.

Claim 4

Baker fails to disclose a data transfer control device comprising a packet assembly circuit wherein the packet assembly circuit updates a control information pointer indicating an address of control information to be read from the control information area when it is determined based on packet format identification information included in the control information of the packet that the control information of the packet is read, and updates a data pointer indicating an address of data that is to be read from the data area when it is determined based on the packet format identification information that the data of the packet is read.

The Office Action asserts that elements 524 and 526 of Baker correspond to data pointers; however Baker is silent about updating control information (header) pointer or data pointer, based on packet format identification information (e.g., tcode) included in the control information of the packet. For example, with reference to Fig. 28 of the present application, when the packet assembly circuit determines, based on the packet format identification formation, that the control information of the packet is to be read, the control information pointer HP is updated (incremented) as shown by B10. In this way, control information H0 to H4 is read from storage. Similarly, when the packet assembly circuit determines, based on the packet format identification formation, that the packet data is to be read, the data pointer H4 is updated (incremented) as shown by B12. In this way, data D0, D1, D2 and so on is read from the storage. Furthermore, as discussed above, the data pointer H4 shown by B11 is obtained from the control information of the control information area as shown in Fig. 30B. Baker fails to disclose these features.

Claims 7-10

Baker does not disclose a data transfer control device which manages an interface with a random accessible storage memory, and further comprising a control information

creating section which creates control information and writes the control information to the control information area, and a transmission start section which instructs a start of transmission of a packet, on condition that both data fetch processing and write processing have been completed, as claimed in claims 7-10.

The Office Action appears to rely on page 17, lines 33+ of Baker for disclosure of these features; however, Baker is silent as to the features discussed above. Instead, as discussed above, Baker appears to be similar to a comparative example as illustrated in Fig. 8 and Fig. 15A of the present application. In Baker, is does not appear possible to send a packet without using a transfer FIFO - a pattern in which the header is created and written by the upper layer (firmware) first, then data is fetched from the application-layer device, and finally the start of transmission is instructed, as shown in Fig. 15A.

In exemplary embodiments of claims 7-10, the control information creation section and the transmission start section are upper layer (firmware). As discussed above, the upper layer (firmware) does the processing for creating the header and writing it to the header area of the RAM, while data is being fetched from the application-layer device to the data area of the RAM (see, for example, Fig. 15B). As such, data may be transferred much faster than in Baker.

* * *

Thus, none of the applied art disclose all of the features of claims 1-10. As such, for at least the reasons discussed above, it is respectfully submitted that claims 1-10 are distinguishable over the applied art. Furthermore, those claims which depend from claim 1 are likewise distinguishable over the applied art for at least the reasons discussed above, as well as for additional features they recite. Accordingly, withdrawal of the rejection is respectfully requested.

Furthermore, new claim 35 is allowable at least for its dependence on claim 1, as well as for additional features it recites. Moreover, it is respectfully requested that withdrawn claim 34 be rejoined and examined because, at least for its dependence on claim 1, it relates to the general inventive concept of claim 1.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

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